

# Apollo MCU

## Errata List

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**Revision 1.0**

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# Silicon Errata for the Apollo MCU (APOLLO512-xxx)

## 1. Introduction

This document is a compilation of detailed Silicon Errata for the Apollo MCU.

## 2. Document Revision History

Rev #	Date	Description
1.0	Mar 2017	Document initial public release - errata removed from datasheet

**Table 1: Document Revision History**

## 3. Errata Summary List

Below is a list of the errata described in this document. The reference number for each erratum is listed along with its description and link to the page where detailed information can be found.

Erratum Number, Title and Page	Affected Silicon Revisions	Resolution Status	Work-around
"ERR001: Reduced Operating Temperature Range of Apollo Revision A3" on page 5	Revision A3	Fixed in A4	None
"ERR002: IO Master Clock Pin on Apollo" on page 6	Revisions A3 and A4	Not fixed	Hardware
"ERR003: ADC OPMODE Supply Voltage Dependency" on page 7	Revisions A3 and A4	Not fixed	Software
"ERR004: ADC Trigger 4 Affects Internal Voltage Rails" on page 8	Revisions A3 and A4	Not fixed	None
"ERR005: POR Rising Slew Rate Limitation" on page 9	Revisions A3 and A4	Not fixed	Hardware
"ERR006: Falling POR Threshold At Cold Temperatures" on page 10	Revision A3	Fixed in A4	Software
"ERR008: I2C Clock Stretching" on page 11	Up to and including A4	Not fixed	Software

**Table 2: Errata Summary**

## 4. Detailed Silicon Errata

This section gives detailed information about each erratum. Information covered for each erratum includes the following:

- **Erratum Reference Number and Title** – Lists reference number and title of the erratum
- **Description** – Provides a detailed description of the erratum
- **Affected Silicon Revisions** – Specifies the silicon revisions on which the erratum exists
- **Application Impact** – Describes the impact of the erratum on a user application
- **Workarounds** – Proposes software or hardware workarounds to minimize or eliminate the risk of the erratum occurring
- **Erratum Resolution Status** – Specifies which silicon revision, if any, that the erratum was initially fixed
- **Ambiqsuite Workaround Status** – Specifies whether the erratum has been worked around in the Ambiqsuite software

## **4.1 ERR001: Reduced Operating Temperature Range of Apollo Revision A3**

### **4.1.1 Description**

Revision A3 Apollo MCU devices are only guaranteed to operate within the -10°C to 60°C temperature range. This range is less than the one shown in the Apollo MCU datasheet of -40°C to 85°C. The reduced range is required to guarantee operation as process and voltage vary in revision A3, in addition to temperature.

### **4.1.2 Affected Silicon Revisions**

This silicon erratum applies to all packages of Apollo silicon revision A3.

### **4.1.3 Application Impact**

Customers must use Apollo revision A3 within the reduced temperature range of -10°C to 60°C.

### **4.1.4 Workarounds**

There is no workaround for this erratum other than to operate the device within the reduced temperature range.

### **4.1.5 Erratum Resolution Status**

A new silicon revision now in production (A4), expands the operating temperature range to the expected values of -40°C to 85°C.

### **4.1.6 Ambiqsuite Workaround Status**

Ambiqsuite requires no workaround for this erratum.

## **4.2 ERR002: IO Master Clock Pin on Apollo**

### **4.2.1 Description**

Apollo MCU devices support configuring each of the two IO Master peripherals in either I<sup>2</sup>C mode or SPI mode. When configured in either mode, the device IO masters may experience issues where a transaction is corrupted.

### **4.2.2 Affected Silicon Revisions**

This errata affects Apollo MCU revision A3 and A4.

### **4.2.3 Application Impact**

The prevalence of this issue depends on a combination of normal device package variation, board trace inductance, capacitive loading of the SCL/SCLK line, and pad drive strength settings.

Under certain conditions, a second clock edge forms on the SCL/SCLK line that is read by the IO Master peripheral, which puts it in an undetermined state, corrupting a normal transaction.

### **4.2.4 Workarounds**

To prevent this issue across all possible board configurations, Ambiq Micro requires that customers place a 100  $\Omega$  resistor in series with the SCL/SCLK pin. This resistor should be placed close to the Apollo MCU device.

### **4.2.5 Erratum Resolution Status**

Not fixed.

### **4.2.6 Ambiqsuite Workaround Status**

None required in software.

### **4.3 ERR003: ADC OPMODE Supply Voltage Dependency**

#### **4.3.1 Description**

The Apollo ADC peripheral includes a mode controller state machine that manages time slot conversions, clock management of the block, and also the power state of its various analog components. The OPMODE bits in the ADC CFG register configure the sample rate mode to be used by the controller. The reset value for the OPMODE field is 0x0, which configures a sample rate less than or equal to 125 kSps. A setting of 0x02 configures the ADC for its highest sample rate of up to 800 kSps but may cause the ADC to not operate correctly at a supply voltage less than 2.0 V.

#### **4.3.2 Affected Silicon Revisions**

This errata affects Apollo MCU revision A3 and A4.

#### **4.3.3 Application Impact**

When the OPMODE bits configure the ADC for the highest sample rate, and the supply voltage of the device is less than 2.0 V, the ADC may not operate correctly.

#### **4.3.4 Workarounds**

Customers must set the OPMODE bits to 0x0 if using the ADC peripheral on Apollo when the supply voltage is less than 2.0 V. This setting guarantees proper operation of the ADC, albeit at a lower sampling rate.

#### **4.3.5 Erratum Resolution Status**

Not fixed.

#### **4.3.6 Ambiqsuite Workaround Status**

Ambiqsuite provides the ability to write to all (writable) register fields. It is the responsibility of the user of the software to conform to the proposed workaround for this erratum by checking the supply voltage level before changing the ADC sample rate setting.

## **4.4 ERR004: ADC Trigger 4 Affects Internal Voltage Rails**

### **4.4.1 Description**

Apollo's ADC can be triggered from nine different sources, eight of which are GPIOs configured as external triggers. Using ADC external trigger 4 (GPIO41), can affect sampling of the VDD input to the ADC due to coupling of the rising edge of the trigger signal. This coupling results in an offset of the ADC measurements of VDD, where the resulting output code is lower than expected. This phenomenon only occurs when using ADC external trigger 4.

### **4.4.2 Affected Silicon Revisions**

This errata affects Apollo MCU revision A3 and A4.

### **4.4.3 Application Impact**

If using ADC external trigger 4 (GPIO41), measurement of VDD will not be accurate.

### **4.4.4 Workarounds**

Ambiq Micro recommends not using ADC external trigger 4.

### **4.4.5 Erratum Resolution Status**

This functionality of GPIO41 has been deprecated in version 1.0 of the Apollo datasheet.

### **4.4.6 Ambiqsuite Workaround Status**

Ambiqsuite does not specifically utilize ADC external trigger 4 in any provided functions, nor do any included examples utilize this trigger. It is the responsibility of the user to avoid using this external trigger if this erratum is of concern.



## **4.5 ERR005: POR Rising Slew Rate Limitation**

### **4.5.1 Description**

Revision A3 Apollo devices require a rising slew rate to be 10 V/s or faster to guarantee that the MCU properly comes out of the reset condition. A voltage supply ramp rate less than 10 V/s may result in the MCU never coming out of reset.

### **4.5.2 Affected Silicon Revisions**

This erratum impacts revision A3 of Apollo devices.

### **4.5.3 Application Impact**

A rising slew rate on the voltage supply to the MCU of less than 10 V/s may not be sufficient to cause the device to come out of reset reliably.

### **4.5.4 Workarounds**

Customers using revision A3 must ensure a 10 V/s or higher ramp rate on the MCU input power supply pins.

### **4.5.5 Erratum Resolution Status**

The following silicon revision, A4, corrects this issue, removing any slew rate requirements for the input supply.

### **4.5.6 Ambiqsuite Workaround Status**

None required.

## 4.6 ERR006: Falling POR Threshold At Cold Temperatures

### 4.6.1 Description

Apollo has a falling edge POR (power-on reset) threshold set to approximately 1.72 V, which will safely reset the MCU state prior to its input power supply falling below the absolute minimum value, which would cause functional failures. While operating the ADC peripheral at cold temperatures, between -10°C and -40°C, it's possible for a system functional failure to occur above this 1.72 V threshold. Operating the ADC at cold temperatures can possibly cause the voltage of an internal supply to drop below 1.72 V, while the supply coming into the chip remains above the threshold.

### 4.6.2 Affected Silicon Revisions

This errata affects Apollo MCU revision A3 and A4.

### 4.6.3 Application Impact

Operating the ADC at very cold temperatures may cause the voltage of an internal supply to drop below 1.72 V, causing a system functional failure.

### 4.6.4 Workarounds

Ambiq Micro recommends using the BOD (brown-out detection) feature, with a threshold set to 2.1 V, to detect a low supply condition at cold temperatures, and disable the ADC in these situations. See Section 11.4 of the Apollo datasheet for more details on using the BOD monitor to detect brown-out events.

### 4.6.5 Erratum Resolution Status

Not fixed.

### 4.6.6 Ambiqsuite Workaround Status

The Ambiqsuite HAL supports setting the BOD level to either 1.8 V or 2.1 V, and the BODH (2.1 V) interrupt to support complying with the workaround of this erratum. It is the responsibility of the user to set the BOD appropriately per operational conditions.

## 4.7 ERR008: I2C Clock Stretching

### 4.7.1 Description

This erratum addresses a limitation in the I2C communication channel in all I2C/SPI Master (IOM) modules on the MCU. The issue concerns the inability of the MCU, acting as an I2C master, to react to an I2C slave's attempt to stretch the clock (SCL). The slave would normally be able to hold the SCL line low on any clock cycle of an I2C data transfer from the master for an unlimited amount of time to stall further master transmission. This would normally be done when the slave is processing the I2C data in order to evaluate the address put on the bus and/or prepare the next byte of data to be sent by the slave to the master. The effect of this erratum is that the master either does not process the data from the slave correctly after a clock stretch or, in some cases, ceases to operate entirely.

### 4.7.2 Affected Silicon Revisions

This issue affects all Apollo silicon revisions up to and including A4.

### 4.7.3 Application Impact

The impact of this erratum is that, without a software workaround, an MCU configured as an I2C master does not react properly to a slave's attempt to stretch the I2C clock. Therefore the MCU may be incompatible with certain I2C slave devices which utilize clock stretching as part of their I2C communication.

### 4.7.4 Workarounds

The hardware workaround for this issue is to ensure that no I2C-connected peripheral in the system requires, or will attempt to employ, clock stretching when the MCU is configured as the I2C master. When possible, peripherals which use SPI as the local bus should be selected instead of those requiring the use of I2C. Alternatively, a bit-bang implementation of an I2C master port can be employed instead of using the MCU's IOM module to communicate with I2C slave devices.

### 4.7.5 Erratum Resolution Status

No fix is scheduled at this time.

### 4.7.6 Ambiqsuite Workaround Status

There is a bit-bang solution for Apollo2 but it has not been backported for Apollo in Ambiqsuite at this time. Consult the Apollo2 Errata List for more information.

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